IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. Remarks

Rejection of Claims 1-20 Under 35 U.S.C. §102(e) based on *Abramovici et al.* (U.S. Patent No. 6,631,487).

The rejection of claims 1-10 will first be addressed.

The invention of amended claim 1 is directed to a programmable logic device (PLD) assembly. The PLD assembly includes a programmable logic circuit that provides functions according to configuration data, including a self-test function. In addition, the PLD assembly includes at least one nonvolatile store of the programmable logic device assembly coupled to the programmable logic circuit that provides self-test configuration data for the programmable logic circuit and subsequently stores user configuration data.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

The reference *Abramovici et al.* is not believed to show or suggest a nonvolatile store in the same PLD assembly as a programmable logic circuit, as recited in claim 1.

Abramovici et al. includes a block diagram showing a field programmable gate array (FPGA) under test 10, a controller 12, and a memory 14. However, the memory is never shown or suggested to be part of the same PLD assembly as a programmable logic circuit.

For this reason alone, this ground for rejection is traversed.

In addition or alternatively, *Abramovici et al.* does not show a nonvolatile store. To show such a limitation, the rejection relies on the following reasoning.

> Means to reconfigure circuit elements, such in circuit elements seen e.g., in Figs. 1-9 as ROM or EEPROM mask read-only memory in a manner clear to those skilled in the art how to partition memory in plural sectors for storing data or self-test data.[1]

Clarification for this rationale is respectfully requested.

Applicants' have reviewed the cited reference in detail, including a word search, and the terms nonvolatile, ROM, and EEPROM are not present in the reference. Applicant requests a

[1] Office action, dated 3/10/04, Page 3, Lines 4-7.

citation to the reference to show where such limitations are shown, either explicitly or inherently.

If the above excerpt represents official notice, Applicant seasonably traverses the statement and requests references in support.

Accordingly, because all limitations of the cited reference are not shown, this ground for rejection is traversed.

Various claims depending from claim 1 include limitations not shown in or suggested by the cited reference.

Claim 4 recites that the at least one nonvolatile store is formed with the programmable logic circuit on a single integrated circuit. While the memory of *Abramovici et al.* does store configuration data for the FPGA, the memory is never shown or suggested to be on a single integrated circuit with the FPGA (argued to correspond to Applicant programmable logic circuit).

> [M]emory 14 for storing the various FPGA operational configurations, as well as, test data, and fault-tolerant functions including their associated fault-tolerant reconfigurations.[2]

For this additional reason, claim 4 is not believed to be anticipated by the cited reference.

Claim 5 recites that, not only is the nonvolatile on the same die as the programmable logic circuit, but the nonvolatile store includes re-programmable circuit elements. Again, this limitation is not shown or suggested by the cited reference. Claim 6 adds that such re-programmable circuit elements includes EEPROM cells. *Abramovici et al.* provides no indication its memory includes programmable circuit elements.

For this additional reason, claims 5-6 are believed to be separately patentable over the cited reference.

Claim 7 recites that self-test reconfiguration data is set by at least one manufacturing process step. The reference teaches away from such a limitation. *Abramovici et al.* is directed to on-line testing of an FPGA, the testing of an FPGA that has finished all manufacturing steps and has been installed in a system. This is reflected in the title of the reference (***ON-LINE*** TESTING OF FIELD PROGRAMMABLE GATE ARRAY RESOURCES), as well as throughout the

[2] *Abramovici et al.*, Col. 6, Lines 7-10.

reference:

> In accordance with the present invention, resources of a field programmable gate array (FPGA) determined to be faulty during testing may now be quickly identified and the remaining FPGA resources reconfigured... to allow its continued operation in a diminished capacity, ***during normal on-line operation of the FPGA***.[3]

The remaining portions of *Abramovici et al.* make numerous other references to on-line testing of the FPGA.

Thus, because the reference does not show, and appears to teach away from self-test configuration data established by at least one manufacturing process step, claim 7 is believed to be separately patentable.

Claim 8 recites at least two separate memories. Such a limitation cannot by shown by the cited teachings of the reference. In particular, claim 8 recites a mask PROM for storing self-test configuration data, and a separate nonvolatile memory for storing user configuration data.

As emphasized above, *Abramovici et al.* teaches one memory. Further, such a memory is never described as being a nonvolatile memory of any sort (i.e., PROM).

Claim 9 recites that the at least one nonvolatile store includes at least two sectors. Further, claim 10 recites that a first such sector is boot sector. Such limitations are not shown or suggested by the cited reference. The word "sector" does not appear in the reference, and booting operations are not described.

Accordingly, the reference is not believed to show all limitations of claims 9 and/or 10, either.

If it is being argued that various limitations of the dependent claims are *inherently* present in the cited reference, the rejection remains insufficient to establish a prima facie case of anticipation. Applicant's stress that cases of inherency still require a factual/technical showing.

> [W]hen an examiner relies on inherency, it is incumbent on the examiner to point to the ***"page and line"*** of the prior art which justifies an inherency theory.

[3] *Abramovici et al.*, Col. 1, Line 63 to Col. 2, Line 3.

Compare *In re Rijckaert*, 9 F.3d 1531, 1533, 28 USPQ 2d 1955, 1957 (Fed. Cir. 1993) (when the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the prior art) (citing *In re Yates*, 663 F.2d 1054, 1057, 211 USPQ 1149, 1151 (C.C.P.A. 1981)).[4]

In light of this, Applicant requests a citation as to where any of the following are shown, explicitly or inherently, in *Abramovici et al.*:

1) a nonvolatile store that provides self-test configuration data;

2) a single die with both a programmable logic circuit and a nonvolatile store that provides self-test configuration data;

3) re-programmable nonvolatile circuit elements in a nonvolatile store that provides self-test configuration data;

4) EEPROM cells in a nonvolatile store that provides self-test configuration data;

5) a nonvolatile store that provides self-test configuration data that is set by one or more manufacturing process steps;

6) a mask PROM that stores self-test configuration data and a separate nonvolatile memory that can store user configuration data;

7) a nonvolatile store that stores self-test configuration data in a first of multiple sectors; or

8) a nonvolatile store that stores self-test configuration data in a boot sector.

For all of these reasons, this ground for rejection is traversed.

The rejection of claims 11-17 will now be addressed.

The invention of claim 17 is directed to a method that includes performing a self-test on a programmable logic circuit of one package according to self-test configuration data in a self-test nonvolatile store of the one package. The method further includes storing user configuration data in a user nonvolatile store if the programmable logic circuit passes the self-test.

[4] Ex parte Schricker, 56 USPQ 2d 1723, 1725 (B.P.A.I. 2000) (unpublished).

Abramovici et al. as noted above, teaches self-test of an FPGA by configuring the FPGA into self-test portions internal portions in a roving fashion. However, as emphasized above in the comments for claims 1-10, the reference is silent as to any memory being included in the same assembly as a programmable logic circuit. In the same fashion, the reference is silent as to a "nonvolatile store of the same package", as recited in claim 11.

Accordingly, the reference does not show all limitations of claim 11, and thus does not anticipate the claim.

In addition or alternatively, the reference does not disclose the step of "storing user configuration data in a user nonvolatile store *if* the programmable logic circuit passes the self-test". In fact, the reference appears to teach away from such an arrangement by disclosing a memory that already stores user configuration prior to any testing. That is, *Abramovici et al.* teaches a memory that stores user configuration data ***regardless*** of any test result:

> [S]torage medium or memory 14 for storing ***the various FPGA operational configurations***, as well as, test data, and fault-tolerant functions including their associated fault-tolerant reconfigurations.[5]

From the above, it is clear that the memory of *Abramovici et al.* simultaneously stores all the FPGA configurations described. Thus, the storage of one type of data (e.g., user configuration) is not conditional on any event (e.g., passing the self-test), as recited in claim 11.

For all of these reasons, the cited reference is not believed to show or suggest all limitations of claim 11, and this ground for rejection is traversed.

Various claims depending from claim 11 are believed to be separately patentable over the cited art.

Claim 12 recites that storing user configuration data includes programming user configuration data in locations that stored self-test configuration data. As noted above, *Abramovici et al.* appears to teach storing all configurations at the same time in a memory. Accordingly, the reference does not show, and is believed to teach away from the limitations set forth in claim 12.

[5] *Abramovici et al.*, Col. 6, Lines 7-10.

Claim 15 recites the step of forming a self-test nonvolatile store on the same die as a programmable logic circuit. As noted in the comments for claim 1, such a limitation is not believed to be shown, either explicitly or inherently, in the cited reference.

Claim 16 recites the step of assembling one die with a programmable logic circuit with another die with a nonvolatile store, into the same package. As noted in the comments for claim 1, such a limitation is not believed to be shown, either explicitly or inherently, in the cited reference.

Claim 17, which depends from claim 16, recites that the package is a multi-chip module. Because *Abramovici et al.* is silent as to any package type, let alone a multi-chip module, the reference cannot show or suggest the limitations of claim 17. For this reason, claim 17 is believed to be separately patentable over the cited reference.

The rejection of claims 18-20 will now be addressed.

The invention of claim 18 is directed to a programmable logic assembly self-test method. The method includes the steps of: storing self-test information in a first nonvolatile store of the assembly that places a programmable logic circuit of the assembly into a self-test configuration, executing a self-test on the programmable logic circuit; and providing user configuration information that places the programmable logic circuit in a user configuration.

As emphasized above, claim 18 recites the step of storing self-test information in a first nonvolatile store of the assembly. To show that such a limitation is not shown in the cited reference Applicant incorporates by reference herein the comments set forth above for claim 1.

Dependent claim 20 recites that the method includes user configuration being stored in a second nonvolatile store that is different than a first nonvolatile store that stores the self-test information. To address this ground for rejection, Applicant incorporates by reference herein the comments above set forth for claim 8, which demonstrate that the reference teaches a single memory, not two different stores.

Rejection of Claims 1-20 based on Applicant's Background Art.

The rejection appears to add additional grounds for rejection, as follows:

> Examiner also notes that claims 1-20 read on Applicant's admitted prior (art) Figs. 8a-c since Figs. 8a-c disclose the limitations of claim 1-20, and that Figs. 2a-c are merely relocating simple elements of the admitted prior (art) Figs. 8a-c. It has been held that mere relocation of parts of an invention involves only routine skill in the art.[6]

This ground for rejection is improper and should be withdrawn.

Applicant addressed this rejection in the previous office action, and so will reiterate the previous comments.

First, the rejection equates FIGS. 2A-2C with Applicant's claims 1-20. This is improper. Applicant's claim language represents the metes and bounds for which patent protection is being sought, not one particular embodiment of Applicant's invention, as is the case for FIGS 2A to 2C. That is, a prior art reference can only anticipate Applicant's claims, not Applicant's drawings.

Second, the rationale relied upon is unrelated to anticipation. In re Japiske, is directed to rationales to support obviousness rejections. Thus, the rationale relied upon cannot support an anticipation rejection. That is, if an invention consisted of the relocation of elements shown in a reference, the invention could not be anticipated by the reference, as such elements would not be "arranged as in the claim". However, as held in In re Japiske, such a relocation of elements might be an obvious variation of a prior art teaching.

Third, the claim language includes clear limitations not shown in the cited reference. Just a few examples are set forth below. With respect to claims 1-10, the following are not shown in FIGS. 8A to 8C.

> From claim 1: "at least one nonvolatile store... that provides self-test configuration data for the programmable logic circuit..."
>
> From claim 7: "...self-test configuration data... set by at least one manufacturing process step..."

[6] Office Action, dated 3/10/04, Page 3, Section 3.3.

From claim 8: "... a mask programmable read-only-memory that stores self-test configuration data and a separate nonvolatile memory..."

From claim 9: "...self-test configuration data is stored in a first sector ..."

Third, with respect to Applicant's claims 1-10, the claim language includes clear

With respect to claims 11-17, the following are not shown in FIGS. 8A to 8C.

From claim 11: "performing a self-test... according to configuration data in a self-test nonvolatile store of the one package..."

From claim 13: "programming user configuration data in locations that stored self-test configuration data..."

With respect to claims 18-20, the following are not shown in FIGS. 8A to 8C.

From claim 18: "storing self-test information in a first nonvolatile store of the assembly...

From claim 20: "user configuration data is stored in a second nonvolatile store that is different than the first nonvolatile store...

For all of these reasons, this ground of rejection is improper and should be withdrawn or is traversed.

Rejection of Claims 1-20 Under 35 U.S.C. §103(a), based on *Sharma et al.* (U.S. Patent No. 5,878,051) in view of *Abramovici et al.*

The rejection of claims 1-10 will first be addressed.

The invention of claim 1 is directed to a programmable logic device assembly. The programmable logic device assembly includes a programmable logic circuit that provides

functions according to configuration data including a self-test function. The assembly further includes at least one nonvolatile store of the programmable logic device assembly coupled to the programmable logic circuit. The nonvolatile store provides self-test configuration data for the programmable logic circuit and subsequently stores user configuration data.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[7]

The requisite motivation for any proposed combination must meet a predetermined threshold in order to establish a prima facie case. That is, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art."

The rejection relies on the following reasoning to combine *Sharma et al.* in view of *Abramovici et al.*:

> [I]t would have been obvious... to modify the procedure in Sharma et al. by including therein embedded self-testing as taught by Abramovici et al., because such a modification would provide the procedure of Sharma et al. with a technique wherein "the need for external tester and human supervision associated therewith is obviated, thereby resulting in reduced testing cost." {See Abramovici et al., col. 3 line 39 et seq.}.[8]

Applicant respectfully requests the basis for this motivation. While *Abramovici et al.* appears to be cited, the above rationale is not from *Abramovici et al.* (nor from the other cited reference *Sharma et al.*). In fact, *Abramovici et al.* teaches away from such a limitation, by teaching an embodiment that includes and external controller.

In the present preferred embodiment, ***an external test and reconfiguration***

[7] MPEP §2143.

[8] See the Office Action, dated 3/10/04, Page 7, last full paragraph.

> ***controller 12 is utilized*** because present commercially available FPGAs do not allow internal access to their configuration memory.[9]

Similarly, the second reference relied upon, *Sharma et al.*, also envisions external control:

> The field-programmable gate array can be configured to include an external test bus port adapted to be coupled to an external test bus. The field-programmable gate array is reconfigurable into at least first and second configurations in response to ***test signals applied to the external test bus port...***[10]

Because the motivation for the proposed combination does not appear to be from the cited references, the motivation is not sufficient to support a prima facie case of obviousness.

If the rejection is relying on official notice, Applicant seasonably traverses this statement and requests the citation of references in support.

Various claims depending from claim 1 are believed to be separately patentable over the cited art.

Claim 8 recites that the at least one nonvolatile store includes a mask programmable ROM that stores self-test configuration data, and a separate nonvolatile memory that can store user configuration data. As noted above, *Sharma et al.* shows a ROM (that is, one nonvolatile memory) that stores all configuration data for the FPGA. The reference never teaches separate nonvolatile memories for self-test configuration data and user configuration data.

As noted in the comments for this claim regarding the rejection based on 35 U.S.C. 102(e), such limitations are not shown in *Abramovici et al.*, either.

Accordingly, because the references do not show all limitations of claim 8, a prima facie case of obviousness has not been established for this claim.

Claim 9 recites that the at least one nonvolatile store includes at least two sectors, and self-test configuration data is stored in a first sector. Claim 10 further specifies that the first sector is a boot sector. Such limitations are not shown in *Sharma et al.* Applicant respectfully request a citation as to where separate sectors storing such configuration are shown in the

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[9] *Abramovici et al.*, Col. 5, Lines 55-57.
[10] *Sharma et al.*, Col. 2, Lines 45-48.

reference. As noted in the comments for these claims regarding the rejection based on 35 U.S.C. 102(e), such limitations are not shown in *Abramovici et al.*, either.

Accordingly, because the references do not show all limitations of claims 9 or 10, the rejection of claims 9 and 10 is traversed for this additional reason.

The rejection of claims 11-17 will now be addressed.

To address this ground for rejection, Applicant incorporates by reference the comments set forth above for claim 1. Namely, that the cited motivation for the proposed combination is not from the references and hence not sufficient to establish a prima facie case of obviousness.

The rejection of claims 18-20 will now be addressed.

To address this ground for rejection, Applicant again incorporates by reference the comments set forth above for claim 1. Namely, that the cited motivation for the proposed combination is not from the references and hence not sufficient to establish a prima facie case of obviousness.

In addition, claim 20 is believed to be separately patentable over the cited art. Claim 20 recites providing user configuration data, where such user configuration data is stored in a second nonvolatile store that is different than the first nonvolatile store.

To address the rejection of this claim, Applicant's incorporate by reference the comments set forth above for claim 8. Namely, that neither cited reference shows or suggests such a two store arrangement.

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Claims 1 and 2 have been amended, not in response to the cited art, but to more clearly describe the invention. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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